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EXAMINER	
WEST, JEFFREY R	

ART UNIT	PAPER NUMBER
2857	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/051,297	WALTER ET AL.	
	Examiner	Art Unit	
	Jeffrey R. West	2857	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 July 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-17,20 and 21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-17,20 and 21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 January 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claim Objections

2. Claim 4 is objected to as being dependent on a cancelled claim. For the purpose of examination, it is assumed that claim 4 depends from claim 1 rather than claim 3. Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 4, 5, 7, 9, 16, 17, 20, and 21 are rejected under 35 U.S.C. 103(a) as

being unpatentable over DE Patent No. 4016922 to Popp in view of U.S. Patent No. 5,416,723 to Zyl and further in view of U.S. Patent No. 5,886,565 to Yasui.

Popp discloses an electrical transducer using a two-wire process (001) comprising an analog sensor that detects a quantity to be measured (009, lines 2-6), an analog end stage which is connected downstream of the sensor at the output end of the transducer (010, lines 32-35 and "13" in Figure 1), a processor circuit (010, lines 26-27 and "7" in Figure 1), wherein the processor circuit is not connected serially between the sensor and the analog end stage so that an analog measurement signal transmission path is realized (Figure 1), the analog end stage converting an output signal of the sensor into an impressed output current with a magnitude which is a measure of the quantity to be measured and is fixed within a range of about 0 to 20 mA, specifically about 4 to 20mA (010, lines 32-36 and Figure 1), the electrical transducer being controlled by the processor circuit (004, lines 1-8).

Popp discloses the analog measurement signal transmission path including an analog scaling unit ("6" in Figure 1), the output signal of the sensor and at least one analog setting value are supplied to the analog scaling unit (010, lines 1-8 and Figure 1), and the output signal of the analog scaling unit is supplied to the analog end stage (Figure 1).

Popp discloses that the analog scaling unit is an analog arithmetic circuit to which as the at least one analog setting value a DC voltage signal is delivered (010, lines 1-11) wherein the analog arithmetic circuit comprises at least one analog

multiplier and at least one sign-evaluating (i.e. adding or subtracting) accumulator acting as an adder and/or subtractor (010, lines 11-19).

Popp discloses a power source that produces a non-zero output current (002, lines 14-16).

Popp discloses that the output signal of the sensor is routed past the processor circuit via the analog signal transmission path (Figure 1) when the processor is inactive for enabling changes in the quantity being measured to be followed while the processor circuit is inactive (004, lines 1-5).

As noted above, the invention of Popp teaches many of the features of the claimed invention and while Popp does teach providing both an analog path and a digital path wherein the digital path includes a microprocessor that is not active during normal measurement operation but only provided to perform corrections (004, lines 1-5), Popp does not explicitly disclose that the processor be shifted temporarily from an awake mode into a sleep mode in which the processor is inactive.

Zyl teaches a loop powered process control transmitter operating at a loop power of between 4 and 20 mA (column 1, lines 5-16) wherein during normal operation of the process control transmitter, the microprocessor circuit is shifted temporarily from an awake mode into a sleep mode in which the processor circuit is inactive (column 2, lines 20-30 and column 3, lines 14-18).

It would have been obvious to one having ordinary skill in the art to modify the invention of Popp to explicitly disclose that the processor be shifted temporarily from an awake mode into a sleep mode in which the processor is inactive, as taught by

Zyl, because the invention of Popp does teach that the microprocessor is inactive during normal transducer operation and Zyl suggests that the combination would have improved the operation of the loop-powered transducer of Popp by complying with the strict power requirement of loop-powered devices (column 2, lines 13-30 and column 4, lines 37-56).

Further, since the invention of Popp does teach providing both an analog path and a digital path wherein the digital path includes a microprocessor that is not active during normal measurement operation but only active to perform corrections (i.e. the duration of the processor activity time is shorter than the duration of the processor inactivity time) and the invention of Zyl teaches that the microprocessor is shifted from an awake mode into a sleep mode, the combination would have provided that the activity time in which the processor circuit is active is shorter than the time that the processor circuit remains in the sleep mode.

As noted above, the invention of Popp and Zyl teaches many of the features of the claimed invention including an analog scaling unit as an analog arithmetic circuit to which as at least one analog setting value a DC voltage signal is delivered from a microprocessor. The invention of Popp and Zyl, however, does not specify how this DC voltage is supplied.

Yasui teaches a reference voltage generating circuit having an integrator that generates a reference voltage using a voltage dividing circuit that divides a voltage supplied from a power source for use by the integrator (abstract).

It would have been obvious to one having ordinary skill in the art to modify the invention of Popp and Zyl to include an active integrator for generating the reference voltage, as taught by Yasui because Yasui suggests a corresponding circuit applicable and needed in the invention of Popp and Zyl in order to generate a reference voltage as well as assuring low power consumption and a stable output characteristic (column 1, lines 44-47).

Further, since the DC voltage signal of Popp and Zyl is generated by the microprocessor, the modification of Popp and Zyl with the control circuit integrator of Yasui would provide an active integrator as part of a control circuit within the processing circuit.

5. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Popp in view of Zyl and Yasui and further in view of U.S. Patent No. 5,714,903 to Bruccoleri et al.

As noted above, the invention of Popp, Zyl, and Yasui teaches many of the features of the claimed invention and while the combination does teach an analog scaling unit including an analog multiplier, the combination does not specify that the multiplier be a single-quadrant multiplier.

Bruccoleri teaches a low-consumption analog multiplier that is a single-quadrant multiplier (column 4, line 66 to column 5, line 3).

It would have been obvious to one having ordinary skill in the art to modify the invention of Popp, Zyl, and Yasui to specify that the multiplier by a single-quadrant

multiplier, as taught by Bruccoleri, because Bruccoleri suggests a corresponding multiplier for use in the invention of Popp, Zyl, and Yasui using a multiplier that would have improved efficiency by lowering current consumption while increasing error compensation (column 4, line 66 to column 5, line 3).

6. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Popp in view of Zyl and Yasui and further in view of U.S. Patent No. 3,805,092 to Henson.

As noted above, the invention of Popp, Zyl, and Yasui teaches many of the features of the claimed invention and while the invention of Popp, Zyl, and Yasui does teach an analog scaling circuit including an analog multiplier, the combination does not specify the makeup of the multiplier.

Henson teaches an electronic analog multiplier comprising a plurality of transistors (abstract) and a plurality of operational amplifiers (column 4, lines 32-38 and Figure 3).

It would have been obvious to one having ordinary skill in the art to modify the invention of Popp, Zyl, and Yasui to specify the makeup of the multiplier, as taught by Henson, because the combination would have provided a suitable multiplier for use in the invention of Popp, Zyl, and Yasui that, as suggested by Henson, would have been suitably biased (column 4, lines 32-38) and operated at high operating speed without normally encountered errors caused by the high speed and/or transistor mismatch (column 2, lines 1-11).

7. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Popp in view of Zyl, Yasui, and Bruccoleri and further in view of U.S. Patent No. 6,057,794 to Takamuki.

As noted above, Popp in combination with Zyl, Yasui, and Bruccoleri teaches many of the features of the claimed invention and while the invention of Popp, Zyl, Yasui, and Bruccoleri, does include an analog scaling unit with an adder, subtractor, and single quadrant multiplier, and further while the combination does include an analog-digital converter as an input to the analog scaling unit, the combination does not specify the makeup of the analog-digital converter.

Takamuki teaches a sigma-delta modulation circuit as part of an analog-digital converter (column 1, lines 6-8) including an analog multiplier, adder, and subtractor (column 10, lines 5-14) with an adder connected through a delay circuit and a converter to the input of a multiplier and an adder and subtractor connected to the output of the multiplier (Figure 5).

It would have been obvious to one having ordinary skill in the art to modify the invention of Popp, Zyl, Yasui, and Bruccoleri to specify that the analog-digital converter as an input to the analog scaling unit comprises an analog multiplier, adders, and subtractor, as taught by Takamuki, because while the invention of Popp, Zyl, Yasui, and Bruccoleri is silent as to the makeup of the an analog-digital converter, Takamuki suggests a corresponding circuit applicable and necessary to implement the converter with improved operation through amplitude control using a small, simple configuration (column 2, lines 25-27).

Although the combination of Popp, Zyl, Yasui, and Bruccoleri provides an analog-digital converter electrically coupled to the analog scaling circuit rather that part of the analog scaling circuit itself, it would have been obvious to one having ordinary skill in the art to provide the A/D converter, and corresponding sigma-delta circuit with multiplier, adders, and subtractor, and the analog scaling circuit as one circuit in order to adhere to space constraints. Further, it has been held that forming in one piece which has formerly been formed in two pieces and put together involves only routine skill in the art (see Howard v. Detroit Stove Works, 150 U.S. 164 (1893)).

8. Claims 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Popp in view of Zyl and Yasui and further in view of U.S. Patent No. 5,207,101 to Haynes.

As noted above, the invention of Popp, Zyl, and Yasui teaches many of the features of the claimed invention and while the invention of Popp, Zyl, and Yasui does teach a circuit connected between the analog scaling unit and the analog end stage for attenuating the sensed signal by performing an average calculation, wherein the attenuating circuit comprises an RC element (Popp, 011, lines 5-20), the combination does not include the specifics of the circuit, specifically, regarding an adjustable time constant.

Haynes discloses a two-wire ultrasonic transmitter comprising a sensor that detects a quantity to be measured (column 2, lines 19-22), an analog end stage, comprising an amplifier circuit, connected downstream of the sensor (Figure 4b,

"52"), a processor circuit, including a processor and drive circuit (column 7, lines 41-42) and an analog measurement signal transmission path (see subsequent circuitry from X1 in Figure 4a), the analog end stage including, between the analog scaling unit and the subsequent analog end stage circuitry, an attenuator comprising an RC element (column 2, lines 58-60 and column 8, lines 52-64), having an adjustable time constant (i.e. adjustable resistor and capacitor values) wherein an error output of the attenuator can be compensate by a control circuit (i.e. comparator with threshold detection) (column 8, line 65 to column 9, line 9).

It would have been obvious to one having ordinary skill in the art to modify the invention of Popp, Zyl, and Yasui to include the specifics of the attenuating circuit, specifically, regarding an adjustable time constant, as taught by Haynes, because the combination would have provided improved transducer operation by allowing modification of the attenuating circuit as desired while, as suggested by Haynes, improving the performance of the transducer of Popp, Zyl, and Yasui by effectively minimizing dead band (column 8, lines 52-64).

9. Claims 14 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Popp in view of Zyl and Yasui and further in view of U.S. Patent No. 5,252,967 to Brennan et al.

As noted above, the invention of Popp, Zyl, and Yasui teaches many of the features of the claimed invention and while the invention of Popp, Zyl, and Yasui

teaches operation in two-wire mode, the combination does not disclose means for operation in three-wire mode.

Brennan teaches a reader/programmer for two and three wire utility data communications system comprising a connector for connection to three or two power supply terminals (column 6, lines 18-25) wherein when a detector means determines that power is supplied to either the three or two power supply terminals, the device automatically switches between two and/or three wire operation modes (i.e. when the device detects a connection to the two-wire port or to the three wire port, the mode is automatically switched) (column 19, line 11 to column 20, line 5).

It would have been obvious to one having ordinary skill in the art to modify the invention of Popp, Zyl, and Yasui to include means for operation in three-wire mode, as taught by Brennan, because Popp, Zyl, and Yasui teaches a transmitter for use in pressure measurement and, as suggested by Brennan, the combination would have provided means for a utility meter, such as a pressure or flow meter, to be used in two or three wire modes thereby increasing the versatility of the device while reducing the burden on the user (column 2, lines 7-32).

Further, since the invention of Popp, Zyl, and Yasui employs sleep-mode in order to adhere to power requirements/deficiencies caused by two-wire systems and describes an embodiment wherein the sleep-mode is only performed during a power deficit (Zyl; column 2, lines 13-36) and Brennan teaches switching between two-wire and three-wire systems, it would have been obvious to one having ordinary skill in the art to keep the processor in wake mode during three-wire operations as it is

conventional in the art that three-wire operation does not suffer from the power constraints of two-wire systems.

Response to Arguments

10. Applicant's arguments with respect to claims 1, 4-17, 20, and 21 have been considered but are moot in view of the new ground(s) of rejection.

The following arguments, however, are noted:

Applicant argues:

> However, even though the processor merely carries out corrective interventions on the analog transmission path that does not mean that it is otherwise inactive. To the contrary, as noted by Examiner, the processor also exchanges digital data with an external communication unit. However, the Examiner incorrectly concludes that this digital data exchange is not during normal measurement and that the "communication is in order to transmit the measured data and therefore the normal measurement must have already been carried out."
>
> This conclusion is erroneous and based on an incorrect interpretation of what is disclosed by Popp because, as can be seen from Fig. 1, the sensor 1 determines the measured values and at the same time converts these parameters into corresponding analog signals. Furthermore, at the same time as the analog signal corresponding to the differential pressure dp is fed to the first input of the combinatorial circuit 6, this signal is also fed to the input of the analog/digital converter 5.3. Since the values are measured continuously by the sensor 1, there does not exist a teme when the measurements "have been completed" as is clear from paragraph [003] of the English translation where the following is stated:
>
> > The invention is based on the objective of developing a measuring transducer of the initially cited type, the continuously delivered output signal of which is also able to follow rapid changes of the parameter to be measured without interruption.
>
> Thus, sensing of the differential pressure dp by the sensor 1, correction of the sensed value by the processor and outputting of the transformed load-independent current at the transducer interface 13 is the normal sensing operation of Popp's transducer as is also reflected in the last sentence of paragraph [0010] of the English translation which states that "output current flowing through the two-wire line 14 immediately follows changes in the

> differential pressure dp." If the processor were to be shifted into a sleep mode, it would be impossible for the processor to exchange digital data with an external communication unit because there would not be any data signals from the processor at the second entrance of the transducer interface 13. Likewise, no corrective interventions on the analog transmission path would be possible. That is, because the measuring transducer interface 13 combines the analog transmission path with the digital transmission path. If the microprocessor were to be in a sleep mode, such a combination would not be possible.

The Examiner asserts that Applicant is referring to the dynamic sensing of Popp to indicate that the processor must be active during normal operation. The Examiner asserts, however, that Popp specifically discloses, in paragraph 004, that the dynamic sensing is carried out on the analog transmission path only and the processor is only for corrections, specifically:

> According to the invention, this objective is attained with the characteristics disclosed in the characterizing portion of the claim. The processing of measuring values for dynamic processes takes place on the analog transmission path only. The processor merely carries out corrective interventions on the analog transmission path.

The Examiner also notes that independent claims 1 and 16 require "during normal operation of the electrical transducer, the processor circuit is shifted temporarily from an awake mode into a sleep mode in which the processor circuit is inactive". This limitation does not indicate that the processor must be in the sleep mode throughout the entire normal operation, but only that the processor is shifted temporarily into a sleep mode during the normal operation. Therefore, if Applicant is arguing that the processor's corrections are performed during normal operation, which the Examiner does not agree, as long as the processor is in a sleep mode while the normal measurement is being performed by the sensor, it is still at least

temporarily in a sleep mode during normal operation, and therefore meets the limitation in question.

Applicant argues:

> Thus, a person of ordinary skill viewing the combined teaching of Popp and Zyl, would consider Zyl's alternative technique of adjusting clock speed as the logical modification to apply to Popp since it is related to and compatible with Popp's concept. However, even if Zyl's primary technique of sending the processor into an inactive sleep mode were to be applied to the process and device of Popp, it would not lead to the present invention but rather would result in a transducer having an analog transmission path and a digital path in which the digital path is operated at a low clock frequency during normal operation and only if there is a power deficit, would the processor be shifted into a sleep mode, the Examiner having ignored Zyl's disclosure of this condition as the triggering factor of use of his sleep mode. Moreover, since the processor is operated at a low clock frequency during normal operation in accordance with Popp's teachings, it is unlikely that the processor would need to be shifted into a sleep mode at all (keeping in mind that Zyl's alternative mode in which the clock rate of the processor is reduced requires no sleep mode), and in any case, the time during which the processor would need to be shifted into the sleep mode would most certainly be much shorter than the time during which it is active, the direct opposite of the present invention.
>
> Moreover, the Examiner's basis for combining of these references is fundamentally flawed not only because of his failure to consider that Zyl's sleep mode is not triggered during normal operating conditions, but rather is used only in the exceptional case of a power deficiency, but it also is flawed because of the errors in his assessment of Popp's disclosure as explained at length above. In this regard, the Examiner's attention is directed to column 6, first full paragraph in which Zyl notes that "the microprocessor must remain fully operative during "real time" operations, a teaching that dictates that the processor of Popp be active for enabling the output current flowing through the two-wire line 14 to immediately follow changes in the differential pressure dp without interruption as quoted above.

The Examiner first asserts that the fact the Zyl teaches both an embodiment employing a low clock frequency and an embodiment employing a sleep mode during a power deficit further lends to the combination of Popp and Zyl since one

having ordinary skill in the art would recognize that Popp discloses a low clock frequency embodiment and Zyl teaches the desirability to not only employ such a low clock frequency but also, in an environment with more serious power constraints, a sleep mode embodiment may be preferred. The Examiner further asserts that this is also suggested by Popp in that that Popp discusses the problems of a variety of power constraints, specifically in paragraph 002:

> The design of such measuring transducers represents a compromise between a high processing speed on one hand and a low energy requirement of the circuit components on the other hand. In other words, a limitation of the maximum energy supplied to the measuring transducer restricts the processing speed of the microprocessor. This leads to the output signals of the measuring transducer being unable to immediately follow rapid changes of the parameter to be measured.

The Examiner further asserts that the invention of Zyl is not included to teach any of the aspects of the analog transmission path or other structural aspects of the claimed limitations, nor for "real time" operations that are performed by Zyl, which consist of energy pluses, sampling, and A/D conversion, especially in light of the fact that the invention of Popp discloses independent A/D converters (Figure 1). Instead, Popp discloses that rather than being active during the entire measurement process, the processor is only active for a short time to "merely carr[y] out corrective interventions on the analog transmission path."

Applicant argues:

> With respect to the subject matter of claims 2 and 3 which is now incorporated into claims 1 and 16, the relevance and applicability of the Yasui patent is questioned. Yasui does not disclose an electrical transducer nor does

> he teach use of an analog arithmetic circuit or active integrator as an actuator for a DC voltage signal or a direct current signal. Instead, Yasui discloses a reference voltage generating circuit for generating a stable reference voltage with low power consumption, which voltage is suitable for use in an integrated circuit. Furthermore, this reference voltage generating circuit is not disclosed as being connected to a processor circuit and to a scaling unit as claimed in the present application. Thus, not only does Yasui not teach or suggest applicants' use of an analog arithmetic circuit or active integrator as an actuator for a DC voltage signal or a direct current signal, but it also lacks a basis for connecting it as an actuator that is connected to both a processor circuit and to a scaling unit. Accordingly, any application of the teachings of Yasui to Popp and Zyl in a manner consistent with his disclosure cannot result in the structure disclosed and claimed herein.

The Examiner first asserts that the invention of Yasui is not included to teach the electrical transducer or a connection between a processor and a scaling unit as the invention of Popp already discloses an electrical transducer using a two-wire process (001) including a connection between a processor ("7" in Figures) and an analog scaling unit ("6" in Figures), wherein the analog scaling unit is an analog arithmetic circuit to which as the at least one analog setting value a DC voltage signal is delivered (010, lines 1-11).

Therefore, while Popp does disclose an analog scaling unit as an analog arithmetic circuit to which as at least one analog setting value a DC voltage signal is delivered from a microprocessor, Popp is silent as to how this DC voltage is supplied.

Yasui then teaches a reference voltage generating circuit having an integrator that generates a reference voltage using a voltage dividing circuit that divides a voltage supplied from a power source for use by the integrator (abstract).

Further, the Examiner asserts that it would have been obvious to one having ordinary skill in the art to modify the invention of Popp and Zyl to include an active integrator for generating the reference voltage, as taught by Yasui because Yasui suggests a corresponding circuit applicable and needed in the invention of Popp and Zyl in order to generate a reference voltage as well as assuring low power consumption and a stable output characteristic (column 1, lines 44-47).

Further, since the DC voltage signal of Popp and Zyl is generated by the microprocessor, the modification of Popp and Zyl with the control circuit integrator of Yasui would provide an active integrator as part of a control circuit within the processing circuit.

Applicant argues

> Relative to the rejection of claims 14 and 15, the Examiner's approach while very imaginative, bears no relationship to what is actually taught by Popp, Zyl and Brennan. In this regard, it is noted that the Examiner has failed to address any of the comments presented by applicants in their preceding response, which comments are hereby incorporated by reference for the sake of brevity, and which comments make it clear that Brennan et al. does not and cannot disclose or suggest the features of claims 14 and 15 because nothing in Brennan et al.'s disclosure could teach having one of three power supply terminals connected to a detector means so that, when a predetermined power supply voltage is applied to the connected one of the power supply terminals, the transducer automatically switches to three- wire operation, and the same is true for having the detector means connected to the processor circuit so as to cause the processor circuit to permanently shift into the awake mode during three-wire operation, as contrasted to the Examiner's proposed provision of a utility meter.

The Examiner first asserts that, in response to Applicant's arguments filed December 29, 2006, the Office Action mailed March 21, 2007, was made non-final and the cited discussion regarding Brennan was changed from:

> Brennan teaches a reader/programmer for two and three wire utility data communications systems including three power supply terminals (i.e. receptacles) (column 6, lines 18-25) wherein upon automatic detection of a predetermined voltage of an interrogation signal at the terminals (column 7, lines 43-55 and column 9, lines 47-49), the measurement device sends a wake-up signal to its microprocessor (column 10, lines 30-37) and based upon the interrogation signal, which powers the device (column 9, lines 26-31), operates in either two or three wire mode (column 9, line 50 to column 10, line 10).

to:

> Brennan teaches a reader/programmer for two and three wire utility data communications system comprising a connector for connection to three or two power supply terminals (column 6, lines 18-25) wherein when a detector means determines that power is supplied to either the three or two power supply terminals, the device automatically switches between two and/or three wire operation modes (i.e. when the device detects a connection to the two-wire port or to the three wire port, the mode is automatically switched) (column 19, line 11 to column 20, line 5).

The Examiner maintains that Bernnan teaches such automatic device connection detection and corresponding mode switching between two and three-wire operation, specifically:

> Upon contact of sensor switch 85 with the surface of the button-like inductive port 7 of two wire local network 43 shown in FIG. 1, the closure of switch 85 indicates to the two wire I/O circuitry 67 that probe/adaptor 9 is in contact with two wire port 7. Two wire port 7 is comprised of one or more turns of wiring. When drive coil 83 is brought into proximity with the coil forming part of port 7, the two coils are inductively coupled to each other.
>
> The closure of sensor switch 85 causes two wire I/O circuitry 67 and microprocessor 64 to be activated for the purpose of either reading or programming any encoded registers connected to the two wire local network 43. It should be noted that reader/programmer 1 may further include a manual trigger

7 (see FIGS. 1 and 8) which is a normally-open switch that can be used to manually activate the two wire or three/fourteen wire I/O circuits 67 and 69 and microprocessor 64. Manual triggering of reader/programmer 1 can be used to override the touch sensitive triggering provided by sensor switch 85 when it is desired to manually activate reader/programmer 1. Manual triggering of reader/programmer 1 also acts a backup in case the touch-sensitive switch 85 should fail for some reason. Although touch-sensitive automatic switching using sensor switch 85 has been described primarily in connection with probe/adaptor 9 and two wire port 7, a touch-sensitive sensor switch of the same type could be employed in connection with port 3 of reader/programmer 1 to enable automatic activation of reader/programmer 1 when connecting to a hard-wired three or fourteen wire receptacle 5, as shown in FIG. 1. (column 19, line 41 to column 20, line 5)

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to Applicant's disclosure.

U.S. Patent No. 4,524,624 to Di Noia et al. teaches a pressure and differential pressure detector and transmitter for use in hostile environments including a detector arrangement comprising an adder, subtractor, and multiplier.

U.S. Patent No. 5,956,663 to Eryurek teaches a signal processing technique which separates signal components in a sensor for sensor diagnostics.

U.S. Patent No. 5,083,091 to Frick et al. teaches a charge balanced feedback measurement circuit.

JP Patent Application Publication No. 04-359399 to Tamura et al. teaches a three-wire signal processor that converts a three-wire signal into a two-wire signal.

U.S. Patent No. 3,948,098 to Richardson et al. teaches a vortex flow meter transmitter that can be used in two-wire or three-wire operation.

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeffrey R. West whose telephone number is (571)272-2226. The examiner can normally be reached on Monday through Friday, 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eliseo Ramos-Feliciano can be reached on (571)272-7925. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jeffrey R. West
Primary Examiner
Art Unit – 2857

October 1, 2007